

QUAD BUFFER/LINE DRIVER; 3-STATE

FEATURES

- Output capability: bus driver
- ICC category: MSI

GENERAL DESCRIPTION

The 74HC/HCT125 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT125 are four non-inverting buffer/line drivers with 3-state outputs. The 3-state outputs (nY) are controlled by the output enable input (nOE). A HIGH at nOE causes the outputs to assume a HIGH impedance OFF-state.

The "125" is identical to the "126" but has active LOW enable inputs.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay nA to nY	$C_L = 15 \text{ pF}$ $V_{CC} = 5 \text{ V}$	9	12	ns
C_I	input capacitance		3.5	3.5	pF
CPD	power dissipation capacitance per buffer	notes 1 and 2	22	24	pF

GND = 0 V; $T_{amb} = 25^\circ\text{C}$; $t_f = t_r = 6 \text{ ns}$

Notes

1. CPD is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = CPD \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz C_L = output load capacitance in pF
 f_o = output frequency in MHz V_{CC} = supply voltage in V
 $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

2. For HC the condition is $V_I = GND$ to V_{CC}

For HCT the condition is $V_I = GND$ to $V_{CC} - 1.5 \text{ V}$

PACKAGE OUTLINES

14-lead DIL; plastic (SOT27)

14-lead mini pack; plastic (SO14; SOT108A)

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 10, 13	$1OE$ to $4OE$	output enable inputs (active LOW)
2, 5, 9, 12	1A to 4A	data inputs
3, 6, 8, 11	1Y to 4Y	data outputs
7	GND	ground (0 V)
14	V _{CC}	positive supply voltage

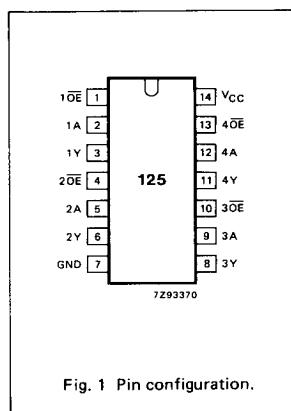


Fig. 1 Pin configuration.

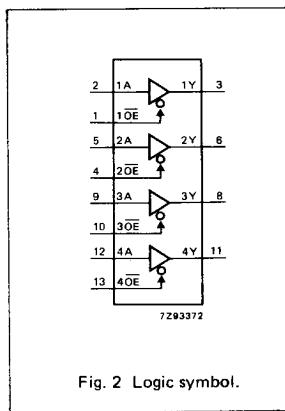


Fig. 2 Logic symbol.

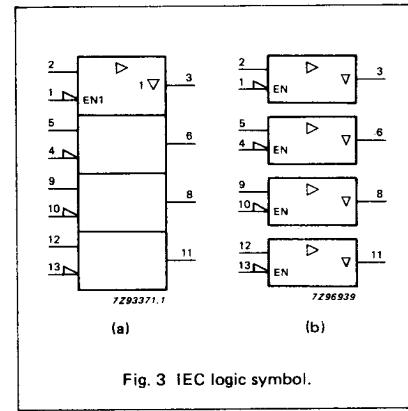


Fig. 3 IEC logic symbol.

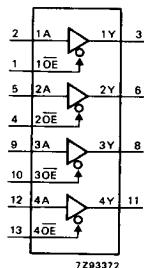


Fig. 4 Functional diagram.

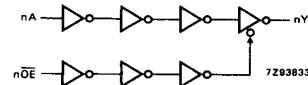


Fig. 5 Logic diagram (one buffer).

FUNCTION TABLE

INPUTS		OUTPUT
nOE	nA	nY
L	L	L
L	H	H
H	X	Z

H = HIGH voltage level

L = LOW voltage level

X = don't care

Z = high impedance OFF-state

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T _{amb} (°C)							UNIT	TEST CONDITIONS				
		74HC								V _{CC} V	WAVEFORMS			
		+25			−40 to +85		−40 to +125							
		min.	typ.	max.	min.	max.	min.	max.						
t _{PHL} / t _{PLH}	propagation delay nA to nY	30 11 9	100 20 17		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 6			
t _{PZH} / t _{PZL}	3-state output enable time nOE to nY	41 15 12	125 25 21		155 31 26		190 38 32		ns	2.0 4.5 6.0	Fig. 7			
t _{PHZ} / t _{PLZ}	3-state output disable time nOE to nY	41 15 12	125 25 21		155 31 26		190 38 32		ns	2.0 4.5 6.0	Fig. 7			
t _{THL} / t _{T LH}	output transition time	14 5 4	60 12 10		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 6			

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nA, nOE	1.00

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T _{amb} (°C)						UNIT	TEST CONDITIONS			
		74HCT							V _{CC} V	WAVEFORMS		
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
t _{PHL} / t _{PLH}	propagation delay nA to nY		15	25		31		38	ns	4.5	Fig. 6	
t _{PZH} / t _{PZL}	3-state output enable time nOE to nY		15	28		35		42	ns	4.5	Fig. 7	
t _{PHZ} / t _{PLZ}	3-state output disable time nOE to nY		15	25		31		38	ns	4.5	Fig. 7	
t _{THL} / t _{TLH}	output transition time		5	12		15		18	ns	4.5	Fig. 6	

AC WAVEFORMS

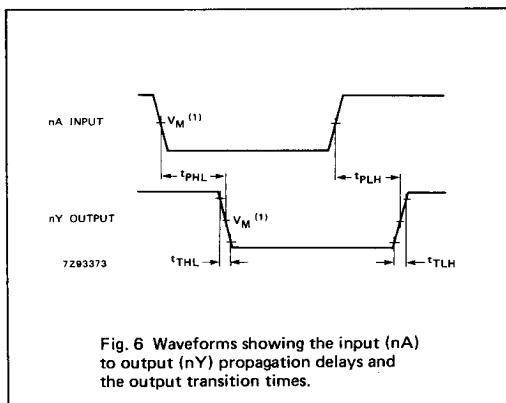


Fig. 6 Waveforms showing the input (nA) to output (nY) propagation delays and the output transition times.

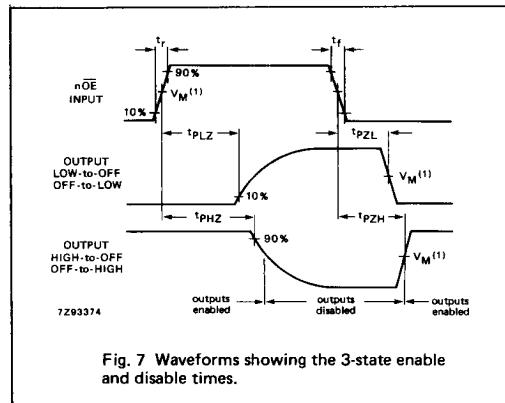


Fig. 7 Waveforms showing the 3-state enable and disable times.

Note to AC waveforms

(1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.
HCT: $V_M = 1.3 \text{ V}$; $V_I = \text{GND to } 3 \text{ V}$.